



UNIVERSIDADE LUSÍADA
LISBOA

Course Unit Program
Computer Architecture

Academic Year 2023/2024

1. Organic Unit

Faculty of Business and Economic Sciences

2. Course

Computer Engineering

3. Cycle

1st

4. Course Unit

Computer Architecture (L9010)

5. Scientific Area

6. Curricular Year

1st

7. Type of Curricular Unit / Semester

2nd Semester



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8. Class type and workload (work time)

Theoretical classes:

Practical classes:

Theoretical-Practical Classes 30,00

Tutorial Guidance: 20,00

9. ECTS Credits

6,00

10. Scientific Area Coordinator

11. Regent

Prof. Doutor BEREND WILLEM MARTIJN KUIPERS

12. Assistants

13. Teaching Language

Portuguese

14. General Objectives

Obtaining knowledge on the internal structures, organization, and algorithms of computers.

15. Specific Objectives

The student will obtain the following know-how:

- (1) Internal structures of computers
- (2) Internal workings of CPUs
- (3) Effect of memory and caching on modern computers
- (4) I/O interfacing from a perspective of a computer

16. Skills to be acquired

The student will obtain knowledge on the fundamental building blocks of computers, its interconnections, as well as, the effect of software to control computers.

17. Teaching Methodology

The classes are taught in oral form, with support of slides. The classes are accompanied by exercises based on the currently taught materials.

18. Course Unit Program



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1. Introduction to the computing system
organization and architecture
structure and function
Historic evolution

2. Numbering systems
decimal system
binary system
hexadecimal system
Conversion between systems
Operations in binary and hexadecimal system
Adders
Representation of numbers in modulus and sign
Representation of numbers in two's complement
Bit multiples in the binary system
Representation of symbols in computing systems

3. Digital logic
Boolean Algebra
logic gates
combinatorial circuits
sequential circuits

4. The von Neumann machine
ENIAC
Structure of the EDVAC - IAS
data and instructions
instruction cycle
run cycle
IAS instructions

5. The computing system
computer components
computer functions
fetching and executing instructions
Interruptions
Operation of I/O modules
bus structure
Hierarchy of buses
Bus design elements
Computer performance metrics
Amdahl's law
Processor performance rating



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Memory performance evaluation

6. Memory systems

Features of memory systems
memory hierarchy

7. Internal memory technologies

DRAM
SRAM
Comparison between DRAM and SRAM memory
ROM
PROM
EPROM
EEPROM~
Flash

8. CACHE memory

Concept
Cach design elements: word, block, label
physical and logical addresses
cache size
Mapping functions: direct, associative, set-associative
Replacement Algorithms: LRU, FIFO, LFU, Random
Write policies: write through, write back
non-cacheable memory
Number of cache memories

9. External memory

magnetic disk
performance parameters
optical memory
magnetic tape

19. Assessment Methods

and according to the University Regulations, the evaluation will have a continuous component and frequency. This course has 3 important topics and the assessment below assesses each of the topics in order to evaluate students on the knowledge obtained by the course.

The continuous component will consist of the following items:

- 2 tests
- TPC

20. Didactic Resources

- data-projector
- CPU simulator running on a PC



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21. Sustainability Objectives

- 4. Quality Education
- 5. Gender Equality
- 9. Industry, Innovation and Infrastructure

22. Keywords

Computers
memory
caching algorithms
assembly programming



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23. Main Bibliography

Author(s): Stallings, William
Title: Computer Organization and Architecture
Edition: 9 Year: 2012
Local:
Publisher: Prentice Hall

Author(s): Delgado, José - Ribeiro, Carlos
Title: Arquitetura de Computadores
Edition: 5ª Year: 2014
Local: Lisboa
Publisher: FCA

Author(s):
Title:
Edition: Year:
Local:
Publisher:

24. Complementary Bibliography

Author(s): Patterson, David A. - Hennessy, John L.
Title: Computer Architecture: A Quantitative Approach
Edition: 5 Year: 2011
Local:
Publisher: Morgan Kaufmann

Author(s):
Title:
Edition: Year:
Local:
Publisher:



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Ficha técnica MIP / MIP Datasheet	
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